

TI C2000 Toolbox Signal Scaling for ADC Sampling in C-HIL Setup

1. Introduction

In a Controller Hardware-in-the-Loop (C-HIL) setup, signals generated in simulation are applied to the controller through the analog outputs (AO) of the HIL device and sampled by the DSP Analog-to-Digital Converter (ADC). Because the **simulation signal range**, **HIL analog output range**, and **DSP ADC input range** are generally different, proper **scaling** and **offset** must be applied to ensure that the DSP reconstructs the original simulated signal correctly.

This document explains the principles behind signal scaling and offset calculation, provides generic formulas, and illustrates their use through practical examples for commonly used Texas Instruments C2000 devices and HIL interfaces.

2. Signal Path Overview

The signal path in a typical C-HIL setup is:

Simulation signal → HIL Analog Output → (Interface Board, optional) → DSP ADC Input

Each stage may impose its own voltage limits or scaling, which must be taken into account when configuring the ADC scaling parameters in the controller software.

3. Factors Affecting Scaling and Offset

The following parameters determine the required scaling and offset:

- **Simulated signal range**
V_sim_min, V_sim_max
Example:
V_sim_min = -60V, V_sim_max = 60V
- **DSP ADC reference voltage range**
V_dsp_min, V_dsp_max

Example (most commonly among TI C2000 devices):

$V_{dsp_min} = 0V$, $V_{dsp_max} = 3V$

Some devices have $V_{dsp_max} = 3.3V$.

- **Interface board scaling** (if used)

Some interface boards include analog scaling or level shifting between the HIL and the DSP. Interface board has its own range in which it propagates a signal from HIL analog outputs to DSP analog inputs:

$V_{interface_min}$, $V_{interface_max}$

If no scaling hardware is present (or no interface board is used), then:

$V_{interface_min} = V_{dsp_min}$,

$V_{interface_max} = V_{dsp_max}$

4. Interface Board Gain (G_v)

The interface board gain (G_v) represents the voltage scaling between the HIL analog output range and the DSP ADC input range:

$$G_v = \frac{V_{dsp_max} - V_{dsp_min}}{V_{interface_max} - V_{interface_min}}$$

If no scaling hardware is present (or no interface board is used), then:

$G_v = 1$

Typical Interface Board Gains

- [HIL TI LaunchPad Interface](#): $G_v = 1$
- [HIL TI uGrid Interface](#): $G_v = 1$
- [HIL TI DSP 180 Interface](#): $G_v = 1$
- [HIL TI DSP Interface \(for TMDSCNCD28335\)](#):

$$G_v = \frac{3-0}{5-(-5)} = \frac{3}{10} = 0.3$$

5. Scaling and Offset Formulas

- **Scaling**

Scaling factor converts the ADC input voltage back into the original simulated signal value:

$$\text{scaling} = Gv * \frac{V_{sim_max} - V_{sim_min}}{V_{dsp_max} - V_{dsp_min}}$$

○ Offset

Offset represents the voltage measured at the HIL analog output that corresponds to **zero** in the simulation:

- For **AC signals**, the offset is typically the **midpoint of the interface board voltage range**: $\frac{V_{interface_max} + V_{interface_min}}{2}$.
- For **DC signals**, the offset is typically equal to $(V_{interface_min})$.

The [ADC \(Generic\)](#) block uses the calculated **scaling** and **offset** to reconstruct the original simulated signal and apply it to its output.

Note: It is generally not recommended to use the full ADC input range for steady-state signals, margin should exist for transients to avoid saturation.

6. DSP ADC Voltage Ranges for Supported Devices

Table below shows reference voltages for ADC on devices that are supported by the toolbox.

NOTE: On some devices, reference voltage (V_{dsp_max}) must be configured manually on the development board itself. More information can be found [here](#).

Device	V_dsp_min	V_dsp_max
LAUNCHXL-F28379D	0 V	3.0 V
LAUNCHXL-F28069M	0V	3.3V
LAUNCHXL-F28P650(DK9)	0V	3.0V
LAUNCHXL-F280049C	0 V	3.3 V
LAUNCHXL-F280039C	0 V	3.3 V
LAUNCHXL-F280025C	0 V	3.3 V
LAUNCHXL-F2800137	0 V	3.3 V
TMDSCNCD28379D	0 V	3.0 V
TMDSCNCD28335	0 V	3.0 V

7. Examples: Scaling a [-60 V, 60 V] AC Signal

- **HIL TI LaunchPad Interface + LAUNCHXL-F28379D ($V_{dsp_max} = 3.0V$)**

- $G_v = 1$
- $scaling = G_v * \frac{V_{sim_max} - V_{sim_min}}{V_{dsp_max} - V_{dsp_min}} = 1 * \frac{60 - (-60)}{3 - 0} = \frac{120}{3} = 40$
- $offset = \frac{V_{interface_max} + V_{interface_min}}{2} = \frac{3 + 0}{2} = 1.5$

- **HIL TI LaunchPad Interface + LAUNCHXL-F280049C ($V_{dsp_max} = 3.3V$)**

- $G_v = 1$
- $scaling = G_v * \frac{V_{sim_max} - V_{sim_min}}{V_{dsp_max} - V_{dsp_min}} = 1 * \frac{60 - (-60)}{3.3 - 0} = \frac{120}{3.3} = 36.3636$
- $offset = \frac{V_{interface_max} + V_{interface_min}}{2} = \frac{3.3 + 0}{2} = 1.65$

- **HIL DSP 180 Interface + TMDSCNCD28379D ($V_{dsp_max} = 3.0V$)**

- $G_v = 1$
- $scaling = G_v * \frac{V_{sim_max} - V_{sim_min}}{V_{dsp_max} - V_{dsp_min}} = 1 * \frac{60 - (-60)}{3 - 0} = \frac{120}{3} = 40$
- $offset = \frac{V_{interface_max} + V_{interface_min}}{2} = \frac{3 + 0}{2} = 1.5$

- **HIL DSP Interface + TMDSCNCD28335 ($V_{dsp_max} = 3.0V$)**

- $G_v = \frac{V_{dsp_max} - V_{dsp_min}}{V_{interface_max} - V_{interface_min}} = \frac{3 - 0}{5 - (-5)} = 0.3$
 - $scaling = G_v * \frac{V_{sim_max} - V_{sim_min}}{V_{dsp_max} - V_{dsp_min}} = 0.3 * \frac{60 - (-60)}{3 - 0} = 0.3 * \frac{120}{3} = 12$
 - $offset = \frac{V_{interface_max} + V_{interface_min}}{2} = \frac{5 + (-5)}{2} = 0$
-

8. Examples: Scaling a [0 V, 60 V] DC Signal

HIL TI LaunchPad Interface + LAUNCHXL-F28379D ($V_{dsp_max} = 3.0V$)

- $G_v = 1$
 - $scaling = G_v * \frac{V_{sim_max} - V_{sim_min}}{V_{dsp_max} - V_{dsp_min}} = 1 * \frac{60-0}{3-0} = \frac{60}{3} = 20$
 - $offset = V_{interface_min} = 0$
-

HIL TI LaunchPad Interface + LAUNCHXL-F280049C ($V_{dsp_max} = 3.3V$)

- $G_v = 1$
 - $scaling = G_v * \frac{V_{sim_max} - V_{sim_min}}{V_{dsp_max} - V_{dsp_min}} = 1 * \frac{60-0}{3.3-0} = \frac{60}{3.3} = 18.1818$
 - $offset = V_{interface_min} = 0$
-

HIL DSP 180 Interface + TMDSCNCD28379D ($V_{dsp_max} = 3.0V$)

- $G_v = 1$
 - $scaling = G_v * \frac{V_{sim_max} - V_{sim_min}}{V_{dsp_max} - V_{dsp_min}} = 1 * \frac{60-0}{3-0} = \frac{60}{3} = 20$
 - $offset = V_{interface_min} = 0$
-

HIL DSP Interface + TMDSCNCD28335 ($V_{dsp_max} = 3.0V$)

- $G_v = \frac{V_{dsp_max} - V_{dsp_min}}{V_{interface_max} - V_{interface_min}} = \frac{3-0}{5-(-5)} = 0.3$
 - $scaling = G_v * \frac{V_{sim_max} - V_{sim_min}}{V_{dsp_max} - V_{dsp_min}} = 0.3 * \frac{60-0}{3-0} = 6$
 - $offset = V_{interface_min} = -5$
-

9. Common Pitfalls and Practical Considerations

ADC Saturation

ADC saturation occurs when the voltage applied to the DSP ADC input exceeds its range $[V_{dsp_min}, V_{dsp_max}]$. In a C-HIL setup, this typically happens due to:

- Incorrect scaling factor (too small scaling, causing reconstructed values to exceed expected range),
- Unexpected transients or startup conditions in simulation,
- Attempting to utilize the full ADC range for steady-state operation.

When saturation occurs, the ADC output clips at its minimum or maximum value, leading to distorted measurements and potentially unstable control behavior. To avoid this:

- Do not design scaling to use the full ADC range during steady-state operation,
- Leave sufficient voltage margin for transients and noise,
- Verify scaling using worst-case simulated signal values.

Incorrect Offset Configuration

An incorrect offset factor causes a systematic measurement error even when the scaling factor is correct. Common symptoms include:

- Non-zero measured value when the simulated signal is zero,
- Asymmetric clipping of positive and negative signal excursions,
- Reduced usable dynamic range of the ADC.

Typical causes include:

- Using a DC-style offset for AC signals (or vice versa),
- Incorrect assumption about the interface board voltage midpoint,
- Mismatch between assumed and actual HIL analog output behavior.

As a rule of thumb:

- **AC signals** should use an offset equal to the midpoint of the interface board voltage range,
- **DC signals** should use an offset equal to the minimum interface voltage.

Always validate the offset by measuring the HIL analog output voltage corresponding to a zero-valued simulated signal.

10. Summary

Correct signal scaling is essential for accurate ADC sampling in C-HIL systems. By accounting for the simulated signal range, interface board gain, and DSP ADC reference voltages, consistent and portable scaling configurations can be achieved across different hardware platforms.
